IN THE CLAIMS:

63. A non-volatile semiconductor memory device comprising:

a plurality of bit lines;

a plurality of word lines insulatively intersecting said bit lines;

a memory cell array comprising a plurality of memory cells coupled to said bit lines and said word lines, each memory cell including a transistor with a charge storage portion;

a plurality of programming circuits coupled to said memory cell array (i) for storing data which define whether or not write voltages are to be applied to respective of said memory cells, (ii) for selectively applying said write voltages to a part of said memory cells, which part is selected according to the data stored in said plurality of programming circuits, (iii) for determining actual written states of said memory cells, and (iv) for selectively modifying said stored data based on a predetermined logical relationship between the determined actual written states of said memory cells and the data stored in said plurality of programming circuits, thereby applying said write voltages only to memory cells which are not sufficiently written to achieve a predetermined written state.

64. The device according to claim 63, wherein said data stored in said programming circuits are initially set to initial data, and then said initial data stored in said programming circuits are modified in accordance with said predetermined logical relationship.

65. The device according to claim 64, wherein said initial data are loaded from at least one input line.

66. The device according to claim 63, wherein said plurality of programming circuits simultaneously determine said actual written states of said memory cells.

67. The device according to claim 63, wherein said data stored in said plurality of programming circuits are modified simultaneously in accordance with said predetermined logical relationship.

68. The device according to claim 63, wherein said programming circuits include means for selectively changing voltages of said bit lines according to said data stored in said programming circuits.

69. The device according to claim 68, wherein said voltages of said bit lines are changed selectively and simultaneously by said means for selectively changing voltages of said bit lines.

70. The device according to claim 63, wherein selective modifying of said data stored in said programming circuits and applying said write voltages to said respective of said memory cells are continued until each memory cell is sufficiently written.

71. The device according to claim 63, wherein modifying of said data stored in said programming circuits and applying said write voltages according to said data stored in said programming circuits are repeated during a limited number of cycles.

72. The device according to claim 63, wherein said programming circuits are arranged on a semiconductor substrate.

73. The device according to claim 72, wherein said programming circuits are arranged adjacent to said memory cell array.

74. The device according to claim 63, wherein each of said programming circuits is connected to a respective one of said bit lines.

75. The device according to claim 63, further comprising a verify-termination detector for detecting whether or not all of said memory cells are sufficiently written in accordance with the modified data in said programming circuits based on said predetermined logical relationship.

76. The device according to claim 75, wherein said verify-termination detector is arranged on a semiconductor substrate.

77. The device according to claim 63, in which said plurality of programming circuits selectively modify said stored data based on said predetermined logical relationship between the determined actual written states of said memory cells after application of write voltages thereto and the actual data stored by said plurality of programing circuits prior to application of said write voltages.

78. The device according to claim 63, wherein said plurality of programming circuits simultaneously apply said write voltages to said part of said memory cells.

79. A non-volatile semiconductor memory device comprising:

a plurality of bit lines;

a plurality of word lines insulatively intersecting said bit lines;

a memory cell array comprising a plurality of memory cells coupled to said bit lines and said word lines, each memory cell including a transistor with a charge storage portion;

a plurality of programming circuits coupled to said memory cell array (i) for storing data which define whether or not write voltages are to be applied to respective of said memory cells, said data being initially set to initial data which are loaded from at least one input line, (ii) for selectively applying said write voltages to a part of said memory cells, which part is selected according to the data stored in said plurality of programming circuits, (iii) for determining actual written states of said memory cells, and (iv) for selectively modifying said stored data based on a predetermined logical relationship between the determined actual written states of said memory cells and the data stored in said plurality of programming circuits, said write voltages applied only to memory cells which are not sufficiently written to produce charge storage in the charge storage portion of each respective insufficiently written memory cell.

80. A system including a non-volatile semiconductor memory device comprising:

a plurality of bit lines;

a plurality of word lines insulatively intersecting said bit lines;

a memory cell array comprising a plurality of memory cells coupled to said bit lines and said word lines, each memory cell including a transistor with a charge storage portion; and

a plurality of programming circuits coupled to said memory cell array (i) for storing data which define whether or not write voltages are to be applied to respective of said memory cells, said data being initially set to initial data which are loaded from at least one input line, (ii) for selectively applying said write voltages to a part of said memory cells, which part is selected according to the data stored in said plurality of programming circuits, (iii) for determining actual written states of said memory cells, and (iv) for selectively modifying said stored data based on a predetermined logical relationship between the determined actual written states of said memory cells and the data stored in said plurality of programming circuits, thereby applying said write voltages only to memory cells which are not sufficiently written to produce charge storage in the charge storage portion of each respective insufficiently written memory cell.

81. The system according to claim 80, wherein said plurality of programming circuits simultaneously determine said actual written states of said memory cells.

82. The system according to claim 80, wherein said data stored in said programming circuits are modified simultaneously in accordance with said predetermined logical relationship.

83. The system according to claim 80, wherein said programming circuits include means for selectively changing voltages of said bit lines according to said data stored in said programming circuits.

84. The system according to claim 83, wherein said voltages of said bit lines are changed simultaneously by said means for selectively changing voltages of said bit lines.

85. The system according to claim 80, wherein selective modifying of said data stored in said programming circuits and applying said write voltages to

said respective of said memory cells are continued until each memory cell is sufficiently written.

86. The system according to claim 80, wherein selective modifying of said data stored in said programming circuits and applying said write voltages to said respective of said memory cells are repeated during a limited number of cycles.

87. The system according to claim 80, wherein said programming circuits are arranged on semiconductor substrate.

88. The system according to claim 87, wherein said programming circuits are arranged adjacent to said memory cell array.

89. The system according to claim 80, wherein each of said programming circuits is connected to a respective one of said bit lines.

90. The system according to claim 80, further comprising a verify-termination detector for detecting whether or not all of accessed memory cells are sufficiently written.

91. The system according to claim 90, wherein said verify-termination detector is arranged on a semiconductor substrate.

92. The device according to claim 63, wherein the array of memory cells includes the plurality of memory cells grouped into blocks of cells wherein the cells within individual blocks are resettable together to a single given threshold level range prior to the programming circuits applying said write voltages to the selective block.

93. The device according to claim 92, wherein the blocks of cells individually contain a number of spare cells, and further wherein the device comprises means for substituting the spare cells of a particular block in place of any defective cells within said particular block.

94. The device according to claim 92, additionally comprising a circuit connected with the blocks of cells to simultaneously reset the threshold levels of cells within a selected two or more blocks to said given threshold level range.

95. The device according to claim 94, wherein the reset circuit includes a tag register associated with individual ones of the blocks such that those blocks having their tag registers set are simultaneously reset while those blocks not having their tag registers set are not reset.

96. The device according to claim 92, additionally comprising means for substituting a redundant block of cells for a defective one of said blocks of cells.

97. The device according to claim 92, wherein said memory device interfaces with a host computer to receive the stored data grouped in magnetic disk drive sectors of data.

98. The device according to claim 63, further comprising a cache memory connected to store hold the stored data prior to it being programmed int said memory cells.

99. A non-volatile semiconductor memory system comprising:

a plurality of memory cells arranged into substantially a matrix pattern to construct a memory cell array, data being electrically erasable from and writable in each of said memory cells;

a plurality of bit lines each connected to said memory cells, each for transmitting a voltage corresponding to data to be written to one of said memory cells in which data are to be written in write mode and for receiving a voltage corresponding to data to be read from one of said memory cells from which data are to be read in read mode;

a plurality of data storing circuits each connected to each of said bit lines, for storing data to be written; in the write mode, the written data controlling voltage of said bit lines; and when data are read for write verify, levels of the data to be written and stored in said data storing circuits being determined, on the basis of the data read from said memory cells to which data have been already written, so that data

can be written in only said memory cells to which data have not been properly written;

a plurality of data detecting circuits each connected to a predetermined number of said data storing circuits, each for detecting data stored in each of said data storing circuits and outputting the detected data when data are read for write verify; and

a write end detecting circuit for receiving output signals outputted by said data detecting circuits and for outputting a write completion signal when all the output signals indicate that data are written properly in said memory cells in which data are to be written.

100. A method for programming a non-volatile semiconductor memory device including a plurality of memory cells, a word line a, plurality of bit lines, and a plurality of data latch circuits, in which said plurality of memory cells are coupled to the word line and are coupled to said plurality of data latch circuits through said plurality of bit lines, the method comprising the following steps of:

storing data of a first logic level or a second logic level into said plurality of data latch circuits;

applying a programming voltage to said word line;

applying a first level voltage corresponding to the first logic level or a second level voltage corresponding to the second logic level to said bit lines in accordance with the level of the data stored in said plurality of data latch circuits, wherein said first level voltage promotes programming of the memory cell and said second level voltage maintains a memory state of any memory cell which has been programmed;

sensing a memory state of one or more given memory cells coupled to respective given data latch circuits in which the data of the first logic level is stored and verifying successful programming of each said one or more given memory cell based on the sensed memory state of said one or more given memory cells;

modifying the level of the data stored in said given data latch circuit or circuits, from the first logic level to the second logic level upon verification of successful programming of said given memory cell; and

stopping application of the programming voltage to said word line if data stored in all of said plurality of data latch circuits are the second logic level.

101. A method according to claim 100, wherein said programming voltage applying step comprises applying a programming voltage which is higher than said first level voltage and said second level voltage.

102. A method according to claim 100, wherein said first level voltage or second level voltage applying step comprises applying the first level voltage which changes a threshold voltage of the corresponding memory cell for programming.

103. A method for programming a nonvolatile semiconductor memory device including a plurality of memory cells, comprising the following steps of:

storing control data which defines whether or not write voltages are to be
applied to respective of said memory cells;

selectively applying said write voltages to a part of said memory cells, which part is selected according to the stored control data;

determining actual written states of said memory cells; and

selectively modifying said stored control data based on a predetermined logical relationship between the determined actual written states of said memory cells and the stored control data, thereby applying said write voltages only to memory cells which are not sufficiently written to achieve a predetermined written state.

104. The method according to claim 103, further comprising a step of initially setting initial control data of said control data stored, and a step of modifying said initial control data in accordance with said predetermined logical relationship.

105. The method according to claim 104, wherein said initially setting step comprises a step of setting control data through at least one input line.

106. The method according to claim 103, wherein said actual written states of said memory cells are simultaneously determined.

107. The method according to claim 103, wherein a selectively modifying step comprises simultaneously modifying control data stored in said plurality of programming circuits in accordance with said predetermined logical relationship.

108. The method according to claim 103, further comprising selectively changing voltages applied to said memory cells according to said stored control data.

109. The method according to claim 108, further comprising selectively and simultaneously changing said voltages of said bit lines applied to said memory cells.

110. The a method according to claim 103, wherein said selectively modifying step is continued until each memory cell is sufficiently written.

111. The method according to claim 103, wherein said modifying and applying step is repeated during a limited number of cycles.